

# BUK75/763R1-40B

TrenchMOS™ standard level FET

Rev. 02 — 16 October 2002

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive TrenchMOS™ technology.

Product availability:

BUK753R1-40B in SOT78 (TO-220AB)

BUK763R1-40B in SOT404 (D<sup>2</sup>-PAK).

### 1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Standard level compatible.

### 1.3 Applications

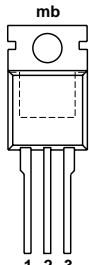
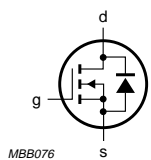
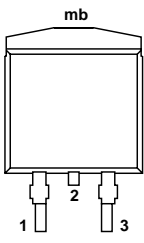
- Automotive systems
- Motors, lamps and solenoids
- 12 V loads
- General purpose power switching.

### 1.4 Quick reference data

- $E_{DS(AL)S} \leq 1.6$  J
- $I_D \leq 75$  A
- $R_{DSon} = 2.6$  m $\Omega$  (typ)
- $P_{tot} \leq 300$  W

## 2. Pinning information

Table 1: Pinning - SOT78 and SOT404, simplified outlines and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)		
		SOT78 (TO-220AB)	
		SOT404 (D <sup>2</sup> -PAK)	

[1] It is not possible to make connection to pin 2 of the SOT404 package.

### 3. Limiting values

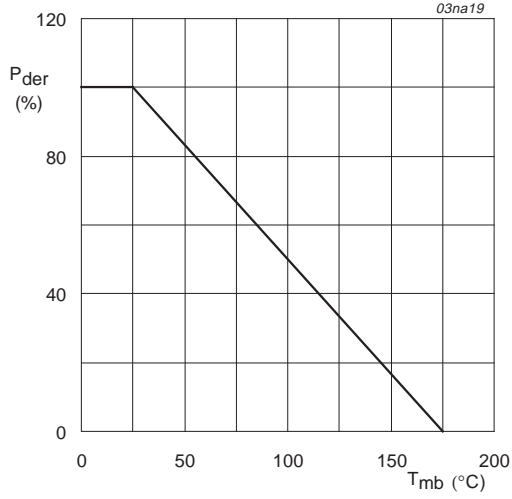
**Table 2: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)		-	40	V
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	40	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 20$	V
$I_D$	drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; $V_{GS} = 10 \text{ V}$ ; Figure 2 and 3	[1] -	225	A
			[2] -	75	A
		$T_{mb} = 100 \text{ }^\circ\text{C}$ ; $V_{GS} = 10 \text{ V}$ ; Figure 2	[2] -	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; Figure 3	-	902	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; Figure 1	-	300	W
$T_{stg}$	storage temperature		-55	+175	$^\circ\text{C}$
$T_j$	junction temperature		-55	+175	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_{DR}$	reverse drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	[1] -	225	A
			[2] -	75	A
$I_{DRM}$	peak reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$	-	902	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75 \text{ A}$ ; $V_{DS} \leq 40 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $R_{GS} = 50 \text{ }\Omega$ ; starting $T_{mb} = 25 \text{ }^\circ\text{C}$	-	1.6	J

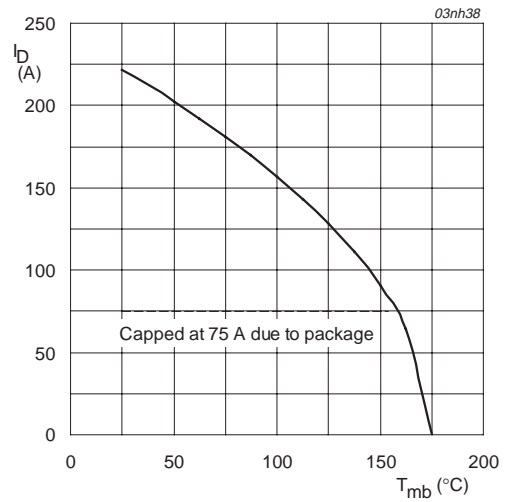
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



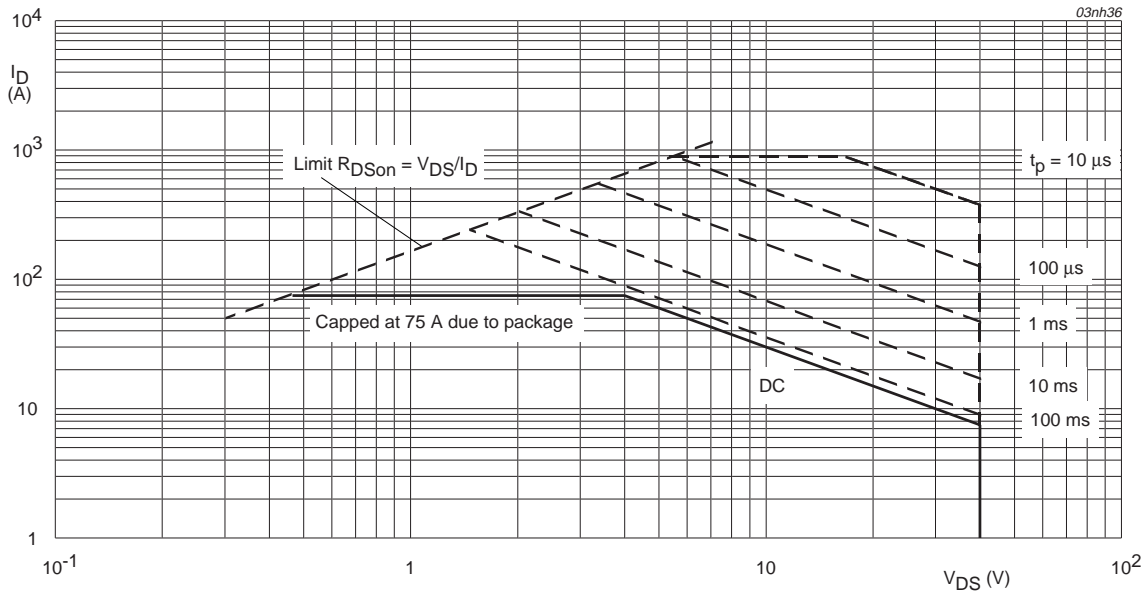
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**



$V_{GS} \geq 10\text{ V}$

**Fig 2. Continuous drain current as a function of mounting base temperature.**



$T_{mb} = 25\ ^{\circ}\text{C}$ ;  $I_{DM}$  single pulse.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

### 4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78 (TO-220AB)	vertical in still air	-	60	-	K/W
	SOT404 (D <sup>2</sup> -PAK)	minimum footprint; mounted on a PCB	-	50	-	K/W

#### 4.1 Transient thermal impedance

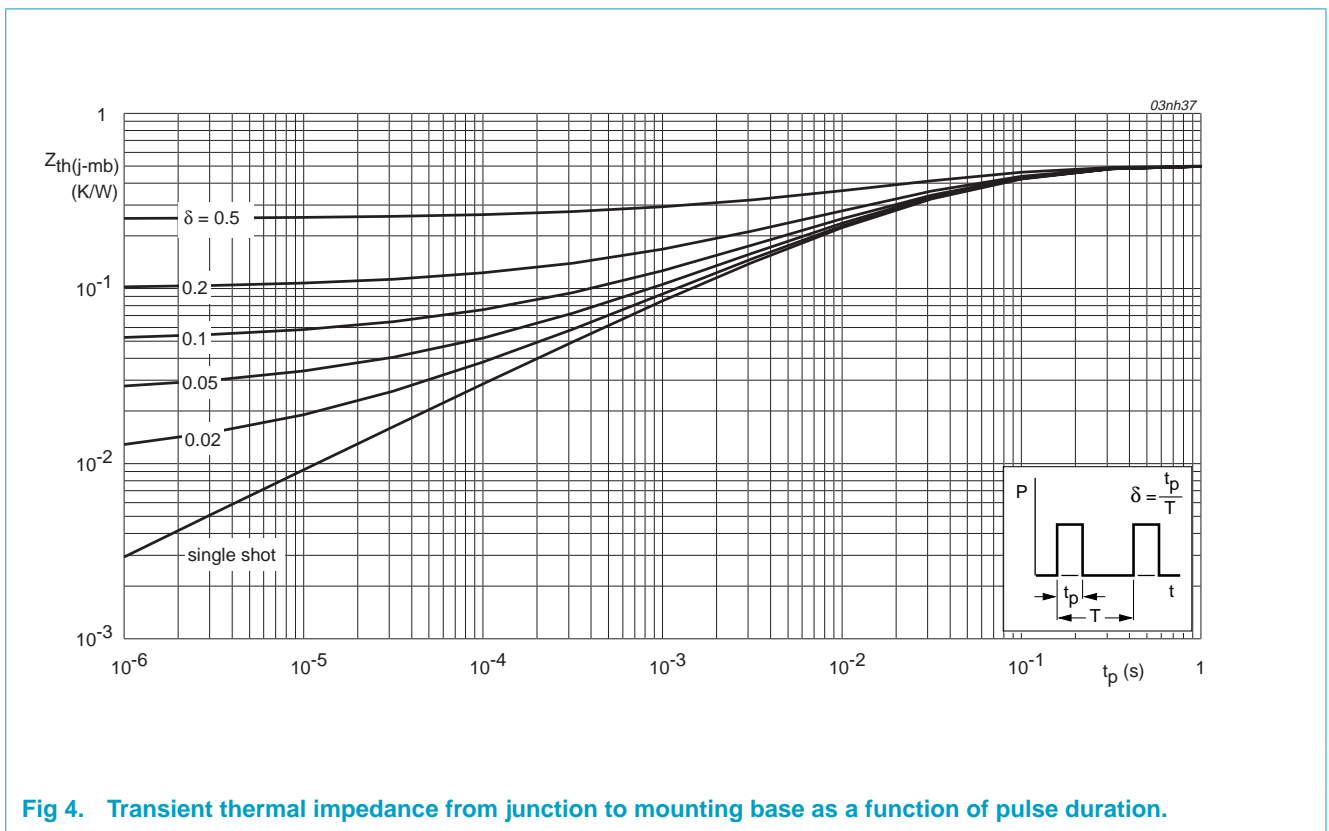


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

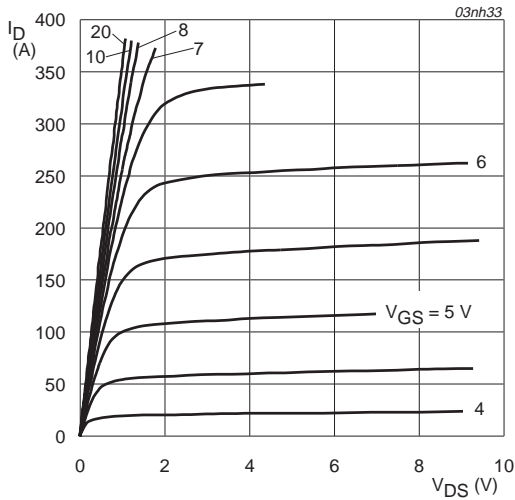
## 5. Characteristics

**Table 4: Characteristics**
 $T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	40	-	-	V
		$T_j = -55\text{ °C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ <b>Figure 9</b>				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 40\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.02	1	$\mu\text{A}$
		$T_j = 175\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ <b>Figure 7 and 8</b>				
		$T_j = 25\text{ °C}$	-	2.6	3.1	m $\Omega$
		$T_j = 175\text{ °C}$	-	-	5.9	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 10\text{ V}; V_{DD} = 32\text{ V};$	-	94	-	nC
$Q_{gs}$	gate-to-source charge	$I_D = 25\text{ A};$ <b>Figure 14</b>	-	18	-	nC
$Q_{gd}$	gate-to-drain (Miller) charge		-	29	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$	-	5106	6808	pF
$C_{oss}$	output capacitance	$f = 1\text{ MHz};$ <b>Figure 12</b>	-	1390	1667	pF
$C_{rss}$	reverse transfer capacitance		-	530	722	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$	-	38	-	ns
$t_r$	rise time	$V_{GS} = 10\text{ V}; R_G = 10\text{ }\Omega$	-	82	-	ns
$t_{d(off)}$	turn-off delay time		-	141	-	ns
$t_f$	fall time		-	90	-	ns
$L_d$	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nH
		from contact screw on mounting base to center of die SOT78	-	3.5	-	nH
		from upper edge of drain mounting base to center of die SOT404	-	2.5	-	nH
$L_s$	internal source inductance	from source lead to source bond pad	-	7.5	-	nH

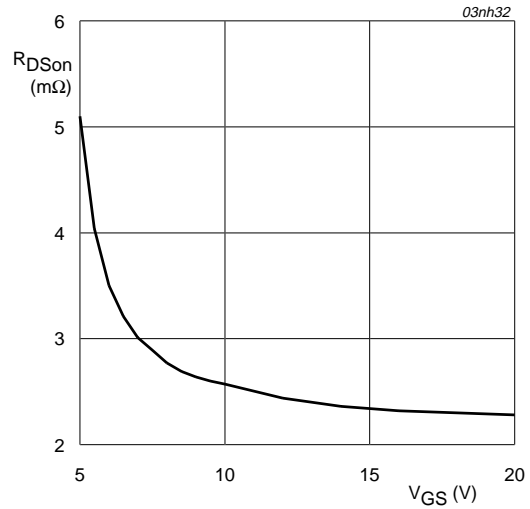
**Table 4: Characteristics...continued***T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 40 A; V <sub>GS</sub> = 0 V; Figure 15	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs	-	65	-	ns
Q <sub>r</sub>	recovered charge	V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 20 V	-	103	-	nC



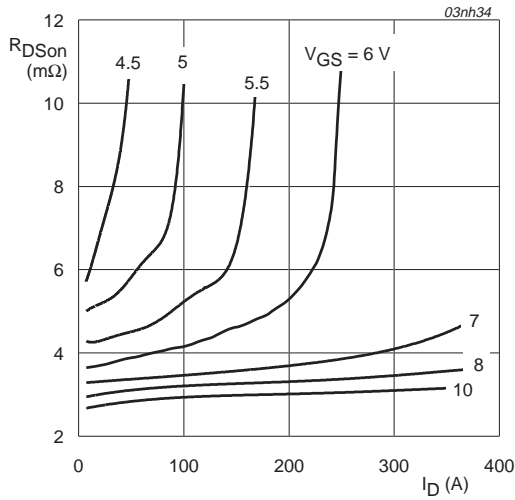
$T_j = 25\text{ }^\circ\text{C}$ ;  $t_p = 300\text{ }\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



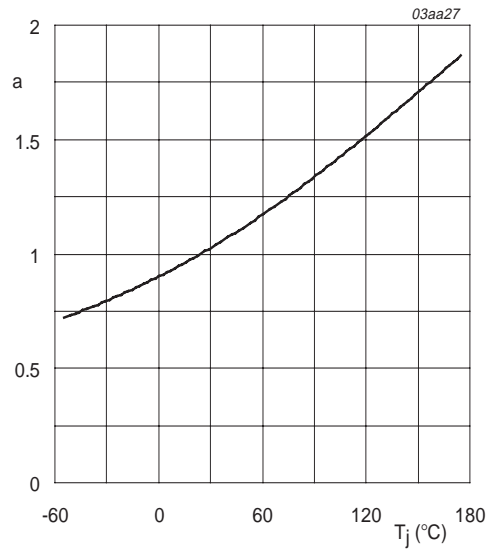
$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 25\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



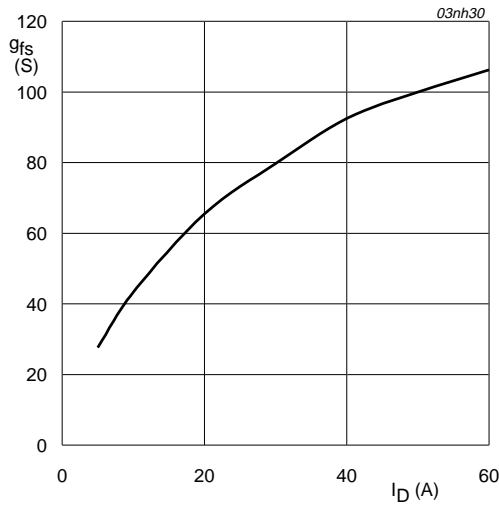
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



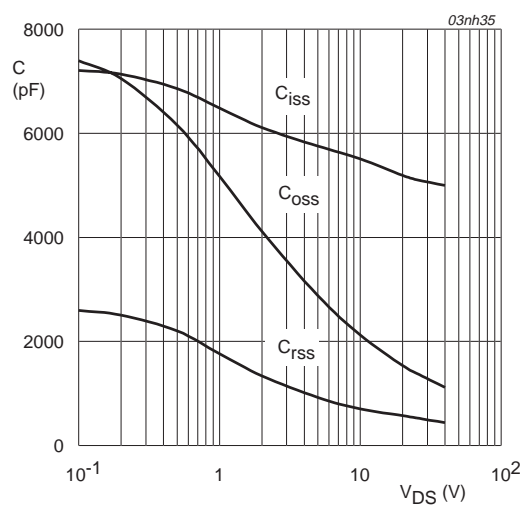
$T_j = 25 \text{ °C}; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



$T_j = 25 \text{ °C}; V_{DS} = 25 \text{ V}$

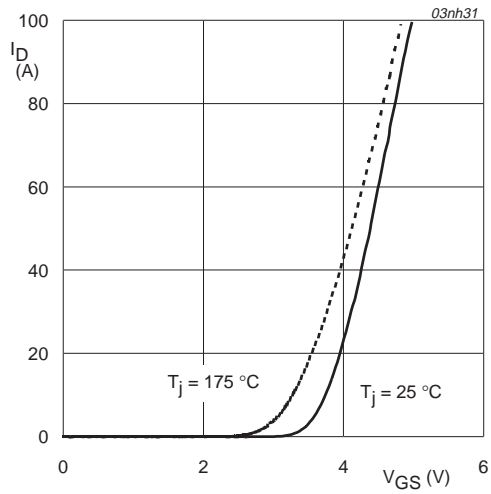
**Fig 11. Forward transconductance as a function of drain current; typical values.**



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

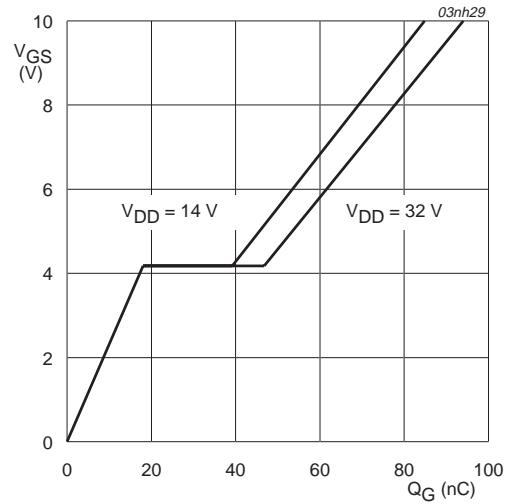
**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**





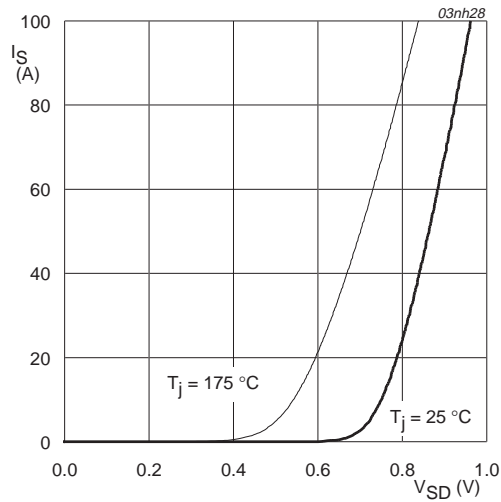
$V_{DS} = 25 \text{ V}$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



$T_j = 25 \text{ °C}; I_D = 25 \text{ A}$

**Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.**



$V_{GS} = 0 \text{ V}$

**Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.**

**6. Package outline**

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

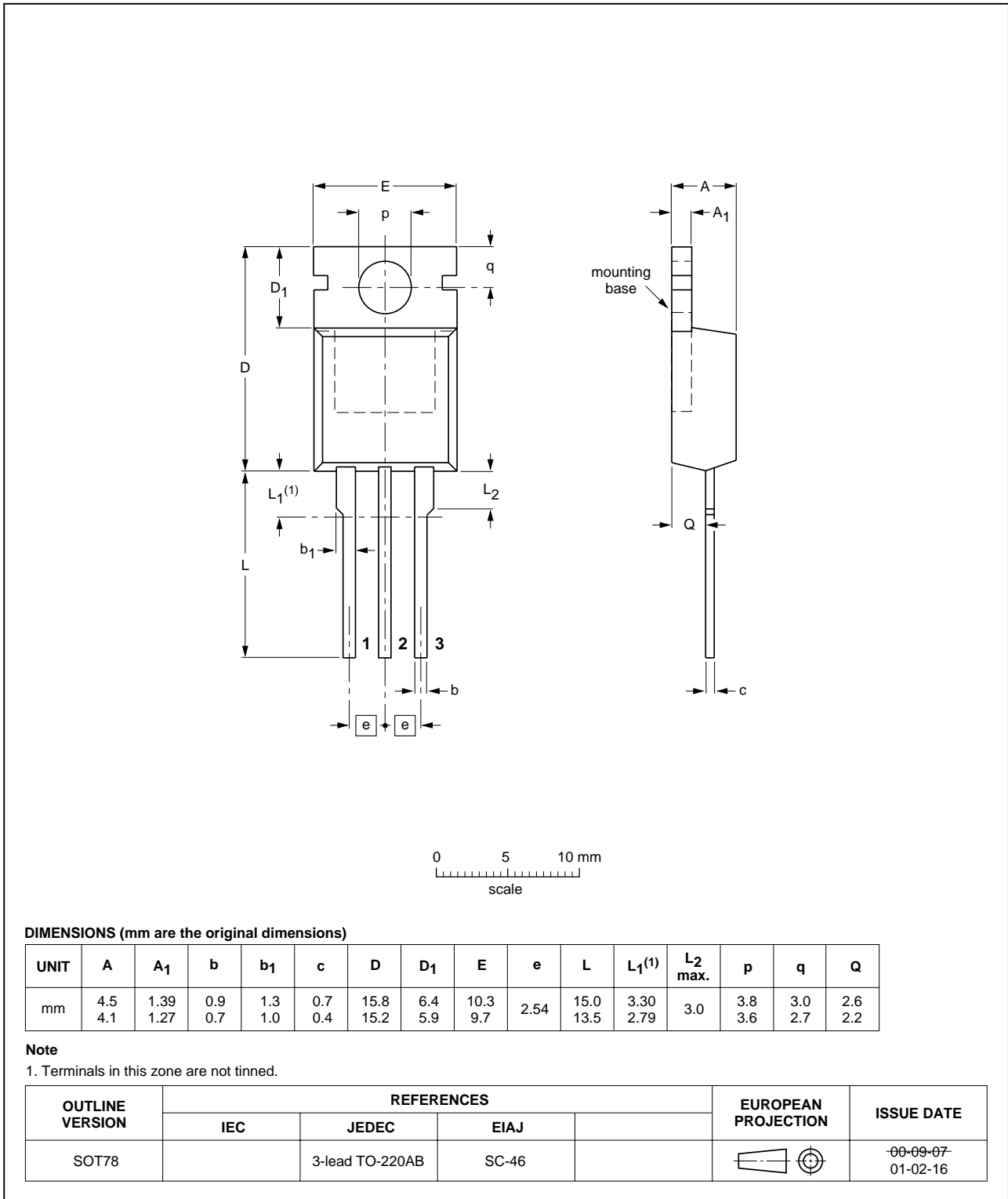


Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404

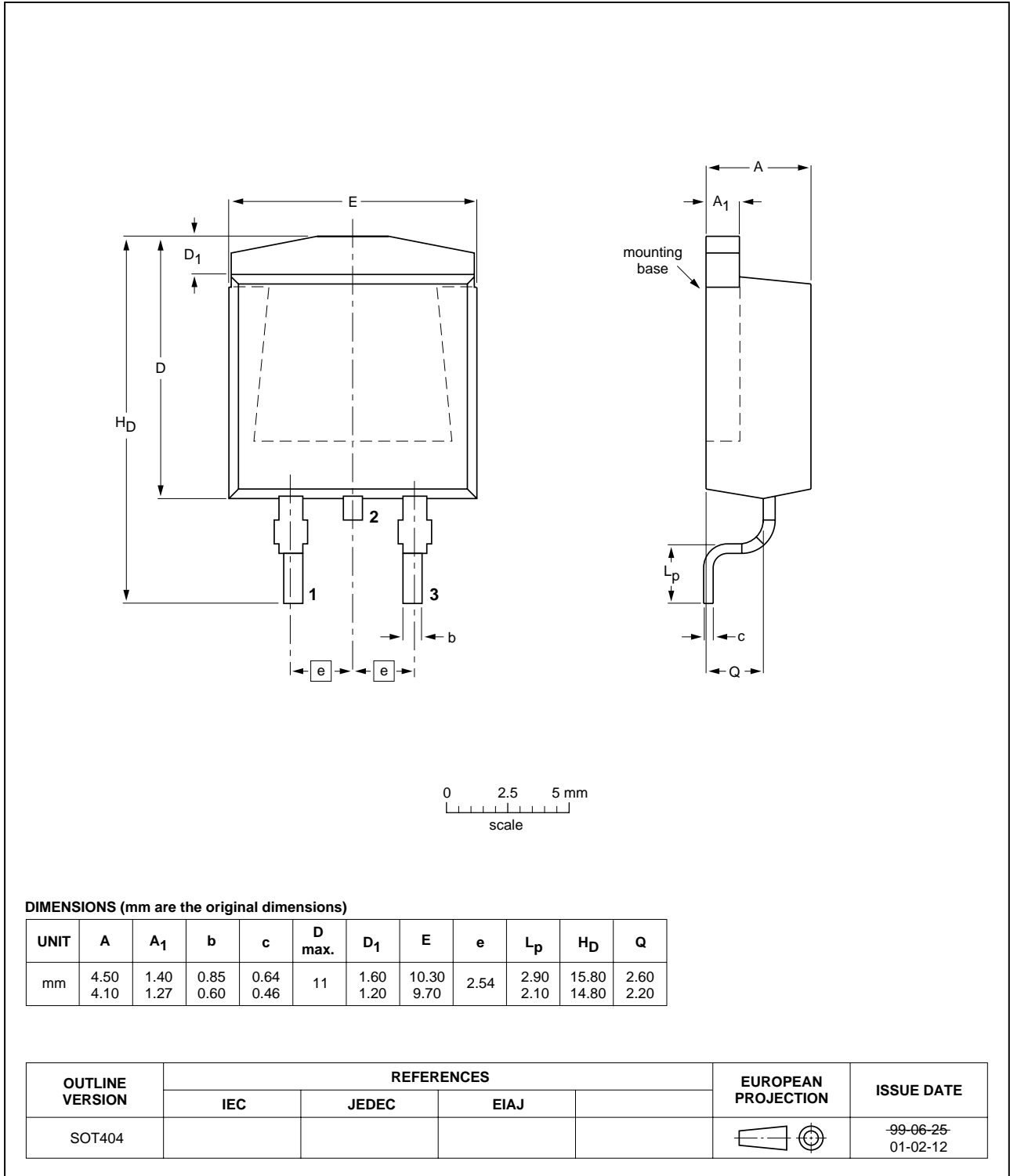
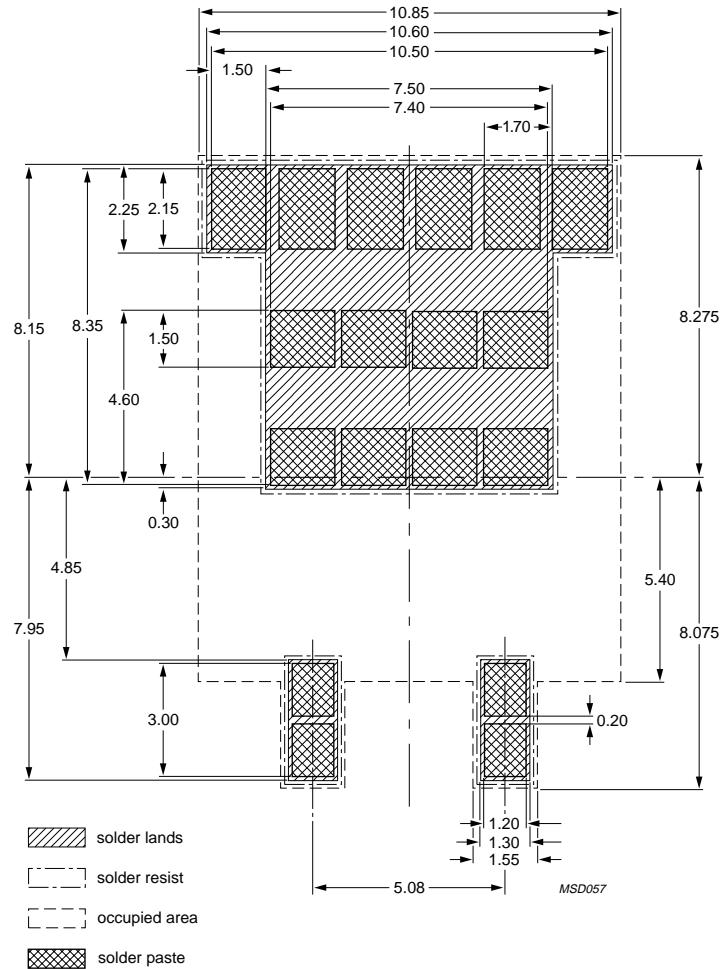


Fig 17. SOT404 (D<sup>2</sup>-PAK)

**7. Soldering**



Dimensions in mm.

**Fig 18. Reflow soldering footprint for SOT404.**

## 8. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
02	20021016	-	<b>Product data; second version; supersedes Rev 01 of 20020409 (9397 750 09489).</b> <ul style="list-style-type: none"><li>Description in <a href="#">Section 1</a> changed from: N-channel enhancement mode field-effect power transistor in a plastic package using generation three TrenchMOS™ technology, featuring very low on-state resistance. to: N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive TrenchMOS™ technology.</li></ul>
01	20020409	-	<b>Product data; initial version.</b>

## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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